Design Methodology and Comparison of Rectifiers for UHF-band RFIDs

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***Abstract*—Rectifiers are important energy converters and henceforth crucial building blocks for RFID applications. In the first half of the work, we have presented a design methodology for matching the rectifier input impedance with the antenna to maximize the rectifier power conversion efficiency. The proposed design approach uses the fundamental transconductance ($Gm(1)$) analysis to estimate the rectifier input impedance. In the second half, a comparison between various possible single-stage rectifier topologies implemented in a CMOS 0.18 μm technology operating at UHF-band is presented. Using voltage conversion efficiency as the FOM, the optimum rectifier topology for RFID application is determined.**

***Index Terms*—CMOS, impedance matching, radio frequency identification (RFID), rectifiers, ultra-high frequency (UHF).**

I. Introduction

Recently there has been an increase in interest in the study and implementation of energy scavenging transceiver architectures for its use in sensor networks, product tags and access control to name a few [1]. The radio frequency identification (RFID) transponder is one such energy scavenging architecture in which the energy storage element (e.g. battery, super capacitor) in the tag is powered up by the transmitted RF signal using a rectifier, also defined as RF-to-DC converter.

To maximize the available power at the energy storage element tag it is necessary to minimize the power loss across the rectifier which is achieved by matching the rectifier input impedance with the antenna [2]. Moreover, using an impedance matching network, tag read-range increases by boosting the available voltage to the rectifier even in cases wherein the available input power is low [3]. Hence, the rectifier power conversion efficiency (PCE) increases as the available voltage to the rectifier increases. However, to select the nature and the values of the components of the matching network an accurate derivation of the rectifier input impedance has to be done through circuit simulator.

The paper discusses the rectifier design methodology to match its impedance to the antenna thereby maximizing the voltage conversion efficiency. In Section II an analysis and design methodology to match the rectifier input impedance with the antenna is described. In Section III a comparison of various rectifier topologies using voltage conversion efficiency as FOM along with experimental results is shown and conclusions are derived thereof.

II. Design Methodology for the Rectifier

To increase the rectifier power conversion efficiency the rectifier impedance is to be matched with the antenna for maximum power transfer. The rectifier input admittance is modeled as a parallel combination of a capacitor and a resistor mathematically represented as $Y_{rec} = G_{rec} + j * Yc_{rec}$, where G_{rec} and Yc_{rec} represents the nonlinear input conductance and susceptance respectively [4]. To match the rectifier input impedance with the antenna (in this case a 50 Ω is considered) the imaginary part is compensated with a parallel inductor (L_p) which is represented by an equivalent series inductance (L_s) as shown in (Fig. 1). A series inductor topology is used to compensate the rectifier capacitive part as it boosts the voltage across the rectifier by a factor "$Q = \omega C_{rec}/G_{rec}$" (which is the resonant structure quality factor) mathematically represented in (1), where V_{AV} corresponds to the input RF voltage as shown in Fig. 1 thereby increasing the voltage conversion efficiency. Once the capacitive part is compensated by the inductor the rectifier nonlinear resistance is matched to 50 Ω by having proper transistor dimensions (W/L ratio).

$$|V_{IN}| = \frac{|V_{AV}|}{2}\sqrt{1+Q^2} \tag{1}$$

In the case of MOSFETs based diode structures to obtain the series inductance value (L_s) it is necessary to compute the rectifier input capacitance which in turn depends on the transistor dimensions for a fixed gate oxide capacitance. The analytical derivation for the rectifier input nonlinear resistance is determined based on the I-V relationship of the MOS device which becomes complicated due to the short channel effects and the quadratic dependency between the current and the voltage. Therefore the aide of large signal analysis in the simulator is used to determine the the rectifier input impedance.

The design procedure for the bridge rectifier shown in (Fig. 2) is described. During the positive cycle of the input RF signal V_{AV} the transistors M4 and M2 are switched on and during the other cycle transistors M3

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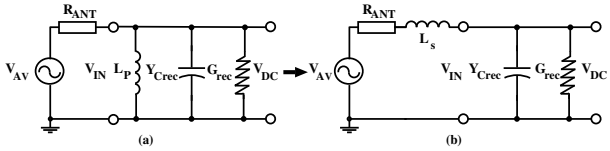

Fig. 1. Simplified schematic of the tag including the antenna, the rectifier equivalent circuit and matching network solutions through an inductor: (a) shunt, (b) series.

and M1 are switched on charging the capacitor C_{OUT} in a single direction thereby rectifying the input RF signal. The input nonlinear resistance determined for a given input

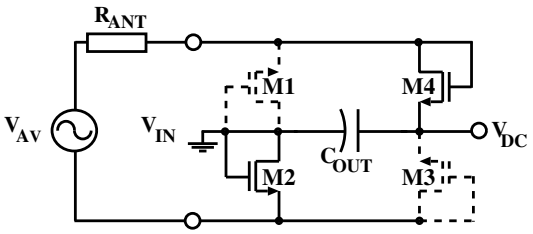

Fig. 2. NMOS bridge rectifier circuit.

power (worst case scenario) using PSS analysis in Cadence simulator for various values of W/L is shown in left hand y-axis of (Fig. 3) and the corresponding value of input capacitance is shown in right hand y-axis of (Fig. 3). From Fig. 3 the input capacitance to achieve 50 Ω is calculated and then the capacitance is compensated by a corresponding series inductance value for the given operating frequency to boost up the voltage across rectifier.

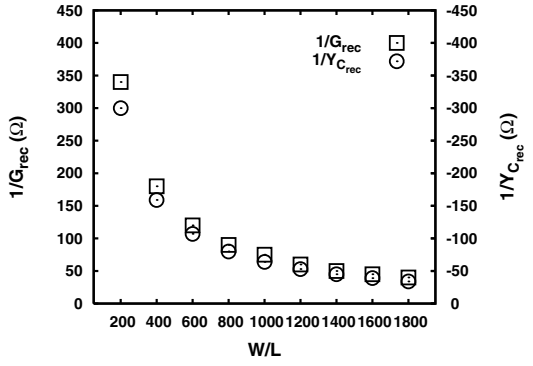

Fig. 3. Simualted nonlinear resistance and input capacitance of the NMOS bridge rectifier.

Fig. 4 compares the rectifier input impedance measured using VNA (Agilent HP8719D) with the results obtained using Cadence Virtuoso simulator. From Fig. 4 it can be seen that the measured value is in good agreement with the simulated value thereby validating the design procedure for the rectifiers.

Fig. 5 shows the measured voltage efficiency as a function of the input available voltage V_{AV}. An off-chip series inductor $L_s = 12\ nH$ was used to boost the input voltage of the rectifier at input RF signal frequency of 900 MHz. From Fig. 5 it can be seen that the rectifier voltage conversion efficiency matched to the antenna is higher in comparison to without series inductor which is as expected. For the calculations, the rectifier voltage conversion efficiency (VCE) is defined as:

$$\eta = \frac{V_{DC}}{V_{AV,p}} \tag{2}$$

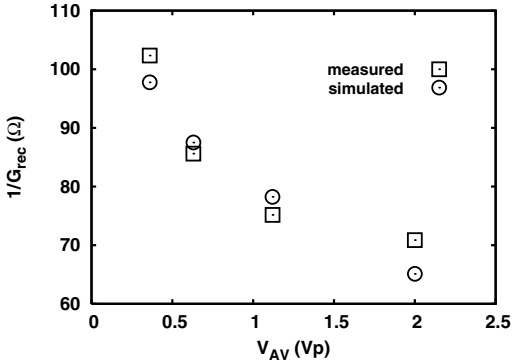

Fig. 4. Simulated and measured real part of the rectifier input impedance with transistor size ratio W/L=500.

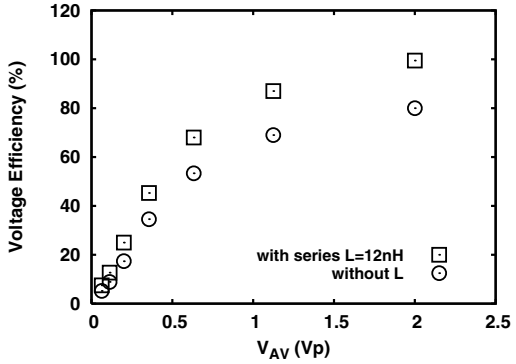

Fig. 5. Comparison between measured DC output voltage of the NMOS bridge rectifier with and without series inductor.

III. Comparison of Rectifiers

In the second half, four rectifier configurations shown in (Fig. 6) are compared using voltage conversion efficiency as the FOM. In general VCE can be improved by cascading several stages but in this paper the idea

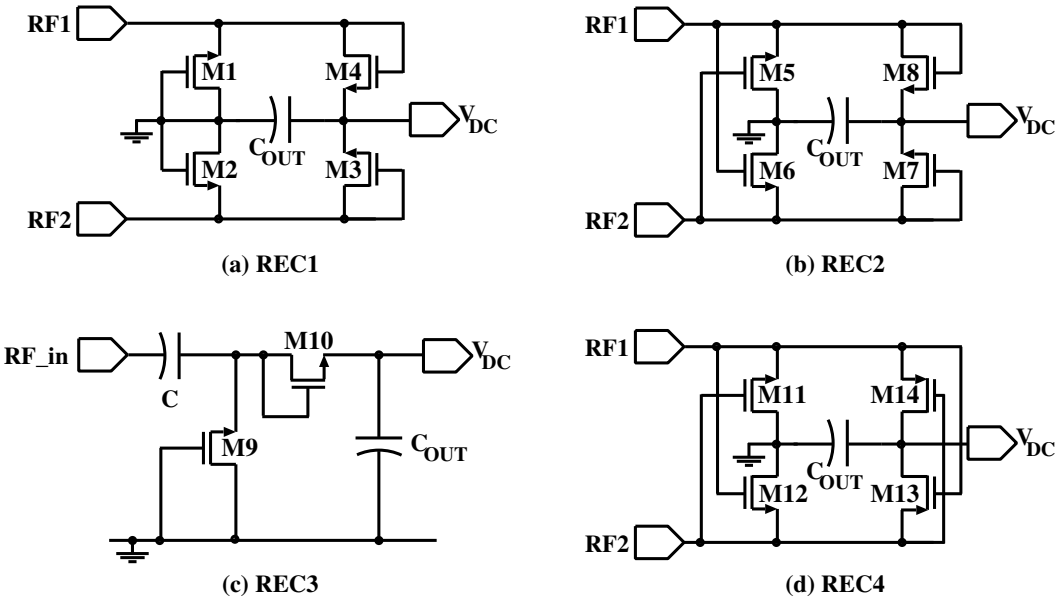

Fig. 6. Rectifier topologies: (a) NMOS differential-drive bridge rectifier, (b) NMOS differential-drive gate cross-connected bridge rectifier, (c) NMOS doubler, (d) NMOS-PMOS differential-drive gate cross-connected bridge rectifier.

is to compare across various rectifier topologies hence a single stage rectifier is used. The rectifier configurations are implemented in CMOS 0.18 μm technology using zero-Vth transistors (Vth=2mV) for NMOS, and low-Vth transistors (Vth=320mV) for PMOS. The use of zero-Vth and low-Vth is to decrease the drop across the transistors and thus increasing the voltage conversion efficiency. A brief description about the operations of various rectifier topologies along with the experimental results is described below.

A. Rec1

Fig. 6.a shows the NMOS differential-drive bridge rectifier normally found in RFID applications where the reader and the tag are in close proximity. For proper rectification using such a topology the input voltage across the rectifiers should be at least twice the threshold voltage, hence using zero-Vth transistors enables such an architecture to operate even at low input power levels.

B. Rec2

Fig. 6.b is a modified version of the common bridge rectifier, where the gate-grounded NMOS transistor are used as switches by cross-coupling each gate thereby decreasing the required input voltage to turn on the transistors and hence an increase in the read range of the RFID tag.

C. Rec3

Fig 6.c is a well known doubler structure where the output V_{DC} ideally is equal to twice the peak input RF voltage. Many such stages can be used in cascade to increase the output voltage hence increasing the overall voltage conversion efficiency.

D. Rec4

Fig. 6.d is similar to Fig. 6.b where the transistors gate input is cross-coupled and hence act as switches. In Fig. 6.d on contrary to Fig. 6.b PMOS transistors are also used and hence al four transistors acts as switches. A major disadvantage of such a topology is the need for a current controlling circuitry as the current direction reverses when the rectified voltage is higher than the input RF voltage.

E. Experimental Results

Fig. 7 shows the photomicrograph of the four rectifiers, fabricated in 0.18 μm CMOS process. The chip was glued on a PCB used for testing the rectifiers. All transitors width and length are 250 μm/0.5 μm, and output capacitor, C_{OUT}, is 5 pF for the bridge converters and 10 pF for the doubler. The input capacitance, C, as in Fig. 6.c has the same value of its output capacitor. Fig. 8 shows the unloaded voltage efficiency of the fabricated single-stage RF-to-DC converters as a function of the available voltage along with a signal frequency of 900 MHz. The VCE increases more than 100% for Rec2 and Rec4, this is the effect yielded by the input voltage boosting due to the series inductor (L_s), whereas for Rec1 and Rec3, VCE increases toward 90%. Fig. 8 can be distinguished into three regions in which for $V_{AV} < 0.5$ V, Rec4 works efficienctly; then, for 0.5 V$\leq V_{AV} \leq$1 V is a transistion

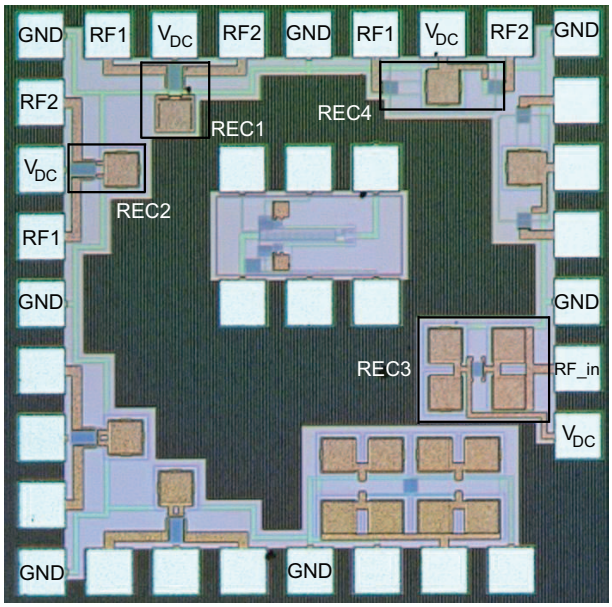

Fig. 7. Photomicrograph of fabricated chip in 0.18 μm CMOS process.

zone between Rec4 and Rec2 and for V_{AV} >1 V, the output DC voltage of Rec2 increases above V_{AV}.

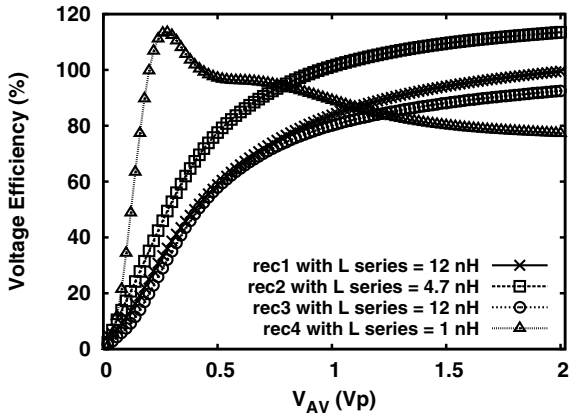

Fig. 8. Measured unloaded voltage efficiency of the RF-to-DC converters fabricated in 0.18 μm CMOS process.

Fig. 9 shows the voltage efficiency of the RF-to-DC converters under different loads with V_{AV} =110 mV at 900 MHz. Even if Rec4 for low input available voltage show the best VCE, in loaded condition its efficiency decreases drastically. Whereas, for the others topologies the VCE is constant until 10 $k\Omega$ and Rec2 clearly has the best loaded voltage efficiency.

IV. Conclusion

A design and comparison methodology for different RF-to-DC converters in UHF-band for RFIDs has been proposed. The input impedance obtained using large signal simulation is compared with the results measured. Four different RF-to-DC converters have been designed and fabricated in 0.18 μm CMOS process. FOM as voltage efficiency has been given to compare the perfomances of the rectifiers. This analysis allows the designer to select the proper rectifier according to its operating condition defined by the available input voltage.

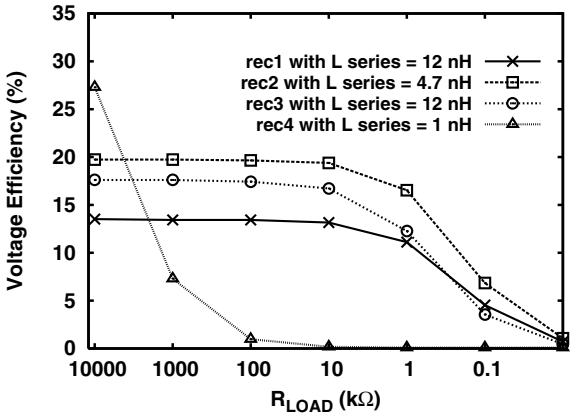

Fig. 9. Measured loaded voltage efficiency of RF-to-DC converters at input available voltage 110 mV.

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